IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A floating gate transistor, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a floating gate opposing the channel region and separated therefrom by a gate oxide, wherein the floating gate includes a vertically ~~horizontally~~ oriented floating gate formed alongside of a body region;

a control gate ~~opposing~~ including a horizontally oriented control gate having at least some portion of the control gate vertically above the floating gate; and

wherein the control gate is separated from the floating gate by a graded, asymmetrical low tunnel barrier intergate insulator formed by multiple atomic layer deposition (ALD).

2. (Previously Presented) The floating gate transistor of claim 1, wherein the asymmetrical low tunnel barrier intergate insulator includes aluminum oxide (Al_2O_3), wherein the aluminum oxide has a number of small compositional ranges such that gradients can be formed by an applied electric field which produce different barrier heights at an interface with the floating gate and control gate.

3. (Original) The floating gate transistor of claim 1, wherein the asymmetrical low tunnel barrier intergate insulator includes an asymmetrical transition metal oxide.

4. (Original) The floating gate transistor of claim 3, wherein the asymmetrical transition metal oxide is selected from the group consisting of Ta_2O_5, TiO_2, ZrO_2, and Nb_2O_5.

5. (Original) The floating gate transistor of claim 1, wherein the asymmetrical low tunnel barrier intergate insulator includes an asymmetrical Perovskite oxide tunnel barrier.

6. (Original) The floating gate transistor of claim 5, wherein the asymmetrical Perovskite oxide tunnel barrier is selected from the group consisting of $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

7. (Original) The floating gate transistor of claim 1, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

8. (Previously Presented) The floating gate transistor of claim 7, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator, wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate.

9. (Original) The floating gate transistor of claim 1, wherein the floating gate transistor includes an n-channel type floating gate transistor.

10. (Currently Amended) A vertical, non volatile memory cell, comprising:

a first source/drain region formed on a substrate;

a body region including a channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the channel region and separated therefrom by a gate oxide, wherein the floating gate includes a horizontally oriented floating gate formed alongside of the body region[[.]];

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by a graded, asymmetrical low tunnel barrier intergate insulator, which is formed by atomic layer deposition (ALD), has a tunneling barrier of less than 2.0 eV, and has a number of small compositional ranges such that gradients can be formed which produce different barrier heights at an interface with the floating gate and control gate.

11. (Original) The vertical, non volatile memory cell of claim 10, wherein the asymmetrical low tunnel barrier intergate insulator includes an insulator selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

12. (Original) The vertical, non volatile memory cell of claim 10, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

13. (Previously Presented) The vertical, non volatile memory cell of claim 12, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the symmetrical low tunnel barrier intergate insulator, wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate.

14.-15. (Canceled)

16. (Previously Presented) A vertical, non volatile memory cell, comprising:

a first source/drain region formed on a substrate;

a body region including a channel region formed on the first source/drain region;

a second source/drain region formed on the body region;

a floating gate opposing the channel region and separated therefrom by a gate oxide;

a control gate opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator, formed by atomic layer deposition (ALD) having a number of small compositional ranges such that gradients can be formed which produce different barrier heights at an interface with the floating gate and control gate;

wherein the floating gate includes a horizontally oriented floating gate formed alongside of the body region.

17. (Previously Presented) The vertical, non volatile memory cell of claim 16, wherein the control gate includes a horizontally oriented control gate formed above the horizontally oriented floating gate.

18. (Currently Amended) A non-volatile memory cell, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide, wherein the floating gate includes a vertically ~~horizontally~~ oriented floating gate formed alongside of a body region;

a first metal layer formed on the polysilicon floating gate;

a metal oxide intergate insulator formed by atomic layer deposition on the metal layer, wherein the metal oxide intergate insulator includes an asymmetrical metal oxide having a number of small compositional ranges such that gradients can be formed in an applied electric field which produce different barrier heights at an interface with the floating gate and control gate;

a second metal layer formed on the metal oxide intergate insulator, wherein the second metal layer has a different work function from the first metal layer; and

a polysilicon control gate formed on the second metal layer.

19. (Previously Presented) A non-volatile memory cell, comprising:

a first source/drain region and a second source/drain region separated by a channel region in a substrate;

a polysilicon floating gate opposing the channel region and separated therefrom by a gate oxide;

a first metal layer formed on the polysilicon floating gate;

a metal oxide intergate insulator formed by atomic layer deposition on the metal layer, wherein the metal oxide intergate insulator includes an asymmetrical metal oxide having a number of small compositional ranges such that gradients can be formed in an applied electric field which produce different barrier heights at an interface with the floating gate and control gate;

a second metal layer formed on the metal oxide intergate insulator, wherein the second metal layer has a different work function from the first metal layer; and

a polysilicon control gate formed on the second metal layer;

wherein the first metal layer includes a parent metal for the asymmetrical metal oxide and the second metal layer includes a metal layer having a work function in the range of 2.7 eV to 5.8 eV.

20. (Original) The non-volatile memory cell of claim 18, wherein the second metal layer is platinum (Pt) and the metal oxide intergate insulator is selected from the group consisting of TiO_2, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

21. (Original) The non-volatile memory cell of claim 18, wherein the second metal layer is aluminum and the metal oxide intergate insulator is selected from the group consisting of Ta_2O_5, ZrO_2, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

22. (Original) The non-volatile memory cell of claim 18, wherein the metal oxide intergate insulator is selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta2O3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

23.–84. (Canceled)

85. (Previously Presented) The floating gate transistor of claim 1, wherein the graded asymmetrical low tunnel barrier intergate insulator includes aluminum oxide having a number of small compositional ranges.

86. (Previously Presented) The floating gate transistor of claim 10, wherein the number of small compositional ranges includes aluminum oxide and is adapted to form gradients in an electrical field to produce different barrier heights at an interface between the floating gate and the control gate.

87. (Previously Presented) The vertical, non volatile memory cell of claim 16, wherein the asymmetrical low tunnel barrier intergate insulator includes an insulator selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

88. (Previously Presented) The vertical, non volatile memory cell of claim 16, wherein the floating gate includes a polysilicon floating gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

89. (Previously Presented) The vertical, non volatile memory cell of claim 16, wherein the control gate includes a polysilicon control gate having a metal layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator, wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate.

90. (Previously Presented) The vertical, non volatile memory cell of claim 16, wherein the number of small compositional ranges includes aluminum oxide and is adapted to form gradients in an electrical field to produce different barrier heights at an interface between the floating gate and the control gate.

91. (Previously Presented) The non-volatile memory cell of claim 19, wherein the second metal layer is platinum (Pt) and the metal oxide intergate insulator is selected from the group consisting of TiO_2, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

92. (Previously Presented) The non-volatile memory cell of claim 19, wherein the second metal layer is aluminum and the metal oxide intergate insulator is selected from the group consisting of Ta_2O_5, ZrO_2, $SrBi_2Ta_2O_3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

93. (Previously Presented) The non-volatile memory cell of claim 19, wherein the metal oxide intergate insulator is selected from the group consisting of Al_2O_3, Ta_2O_5, TiO_2, ZrO_2, Nb_2O_5, $SrBi_2Ta2O3$, $SrTiO_3$, $PbTiO_3$, and $PbZrO_3$.

94. (Previously Presented) The non-volatile memory cell of claim 19, wherein the floating gate transistor includes a vertical floating gate transistor.

95. (Previously Presented) The non-volatile memory cell of claim 19, wherein the number of small compositional ranges includes aluminum oxide and is adapted to form gradients in an electrical field to produce different barrier heights at an interface between the floating gate and the control gate.

96. (Previously Presented) The floating gate transistor of claim 1, wherein the asymmetrical low tunnel barrier intergate insulator is continuously graded.